features, integers, steps, operations, elements and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups thereof.

[0085] Unless described otherwise herein, "depositing" may include any now known or later developed techniques appropriate for the material to be deposited, including, but not limited to: CVD, LPCVD, PECVD, semi-atmosphere CVD (SACVD), high density plasma CVD (HDPCVD), rapid thermal CVD (RTCVD), ultra-high vacuum CVD (UHVCVD), limited reaction processing CVD (LRPCVD), metalorganic CVD (MOCVD), sputtering deposition, ion beam deposition, electron beam deposition, laser assisted deposition, thermal oxidation, thermal nitridation, spin-on methods, physical vapor deposition (PVD), atomic level deposition (ALD), chemical oxidation, molecular beam epitaxy (MBE), plating or evaporation. Any references to "poly" or "poly silicon" should be understood to refer to polycrystalline silicon.

[0086] Any use of the terms "connected," "coupled" or variants thereof should be interpreted to indicate any such connection or coupling, direct or indirect, between the identified elements. As a non-limiting example, one or more intermediate elements may be present between the "coupled" elements. The connection or coupling between the identified elements may be, as non-limiting examples, physical, electrical, magnetic, logical or any suitable combination thereof in accordance with the described exemplary embodiments. As non-limiting examples, the connection or coupling may comprise one or more printed electrical connections, wires, cables, mediums or any suitable combination thereof.

[0087] Generally, various exemplary embodiments of the invention can be implemented in different mediums, such as software, hardware, logic, special purpose circuits or any combination thereof. As a non-limiting example, some aspects may be implemented in software which may be run on a computing device, while other aspects may be implemented in hardware.

[0088] The foregoing description has provided by way of exemplary and non-limiting examples a full and informative description of the best method and apparatus presently contemplated by the inventors for carrying out the invention. However, various modifications and adaptations may become apparent to those skilled in the relevant arts in view of the foregoing description, when read in conjunction with the accompanying drawings and the appended claims. However, all such and similar modifications will still fall within the scope of the teachings of the exemplary embodiments of the invention.

[0089] Furthermore, some of the features of the preferred embodiments of this invention could be used to advantage without the corresponding use of other features. As such, the foregoing description should be considered as merely illustrative of the principles of the invention, and not in limitation thereof.

1. A semiconductor device comprising:
a substrate;
a borderless contact comprised of a metal;
a gate structure on the substrate;
a first spacer disposed between the gate structure and the borderless contact and comprised of a first spacer material;
an interlevel dielectric that at least partially overlies the gate structure; and
a second spacer disposed between at least a portion of the gate structure and the interlevel dielectric and comprised of a second spacer material that is different from the first spacer material.

2. The semiconductor device of claim **1**, further comprising a third spacer disposed on the gate structure and between the interlevel dielectric and the borderless contact.

3. The semiconductor device of claim **1**, further comprising a fourth spacer disposed between the gate structure and the first spacer, where the fourth spacer comprises an inner spacer and the first spacer comprises an outer spacer.

4. The semiconductor device of claim **1**, where the first spacer comprises a nitride and the second spacer comprises a low-k dielectric material.

5. The semiconductor device of claim **1**, where the semiconductor device comprises a metal oxide semiconductor field effect transistor.

6. A method to fabricate a semiconductor device having a borderless contact comprising:
forming a first gate structure on a substrate;
depositing an interlevel dielectric over the first gate structure;
planarizing the interlevel dielectric to expose a top surface of the first gate structure;
removing at least a portion of the first gate structure;
forming a second gate structure in place of the first gate structure;
forming a contact area for the borderless contact by removing a portion of the interlevel dielectric; and
forming the borderless contact by filling the contact area with a material comprised of a metal.

7. The method of claim **6**, where the first gate structure comprises a dummy gate structure and where removing the at least a portion of the first gate structure comprises removing substantially all of the dummy gate structure.

8. The method of claim **6**, where the removed portion of the first gate structure comprises a first cap layer of the first gate structure.

9. The method of claim **7**, where forming the second gate structure comprises forming a layer of silicide and forming a second cap layer.

10. The method of claim **7**, where forming the second gate structure comprises forming a fully silicided gate structure.

11. The method of claim **10**, where the first gate structure comprises a layer of dielectric material overlying the substrate, a layer comprised of polycrystalline silicon overlying the layer dielectric material and the first cap layer overlying the layer comprised of polycrystalline silicon.

12. The method of claim **10**, where forming the second gate structure comprises forming a second cap layer overlying the fully silicided gate.

13. The method of claim **6**, where forming the contact area for the borderless contact comprises depositing a second layer of interlevel dielectric and planarizing the second layer of interlevel dielectric.

14. The method of claim **6**, where the interlevel dielectric comprises an oxide with a nitride liner.

15. The method of claim **6**, where the semiconductor device comprises a metal oxide semiconductor field effect transistor.